DSG-NPS R&D Meeting

Date: October 20, 2020
Time: 11:00 – 12:00

Attendees: Mary Ann Antonioli, Peter Bonneau, Aaron Brown, Pablo Campero, Brian Eng, George Jacobs, Mindy Leffel, Marc McMullen, Amrit Yegneswaran

1. CSS screen development status
    - 1.1. New numbering scheme (scheme 2) for PMTs.
        - 1.1.1. Channels will be numbered from 0 to 35 (bottom-to-top) and columns from 0 to 29 (left-to-right); confirmed with Brad Sawatzky
        - 1.1.2. Mary Ann Antonioli will change the numbering schemes for the main NPS and PMT Settings screens
    - 1.2. Equation to calculate PMT position # or crystal # based on HV slot and channel number is as follows:
      PMT pos # ≡ Crystal # = n x 36 + m; slot # $n \in [0, 29] \wedge$ channel # $m \in [0, 35]$
    - 1.3. Enabled each entry field on the PMT Settings screen with confirmation message "Are you sure you want to do this?"
        - 1.3.1. Will continue to research including "OK" button that confirms both entries at same time
    - 1.4. Aaron Brown will continue researching possibility of using CSS macros and scripts to programmatically place widgets

2. CAEN PV discussion
    - 2.1. Reviewed CAEN HV channel PV list and identified all PVs currently being used to generate CSS-BOY screens
        - 2.1.1. Will go over PV list with Brad Sawatzky during next NPS meeting

3. CAEN testing and data analysis
    - 3.1. George Jacobs has six modules left to analyze for current stability
    - 3.2. Repairs completed by Marc McMullen on the Radiall 52 connector for the Radiall 52-to-SHV adapter designed by DSG, and on connector pins for six CAEN HV modules
    - 3.3. George Jacobs completed 16 of 34 current trip tests in *hvcaentest2*
        - 3.3.1. Ramp up and down rate for trip tests is currently 250 V/s; will decrease ramp rates to 50 V/s to try and avoid two voltage values with same timestamp
    - 3.4. Continuing to look for solutions for XY Plot time being set to UTC
    - 3.5. Developing Python analysis package for trip test data analysis, focusing on plotting current instead of voltage

4. Hardware Interlock System development
    - 4.1. Peter Bonneau is researching hardware readout systems for the Keysight model 34980A temperature scanning system

5. Cable fabrication
    - 5.1. Mindy Leffel has fabricated 930 of 1100 HV divider cables